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(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
20 June 2002 (20.06.2002)

PCT

(10) International Publication Number
WO 02/49248 A2

(51) International Patent Classification[7]: H04J 3/04, H04L 7/033

(21) International Application Number: PCT/US01/48696

(22) International Filing Date:
12 December 2001 (12.12.2001)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/737,668 14 December 2000 (14.12.2000) US

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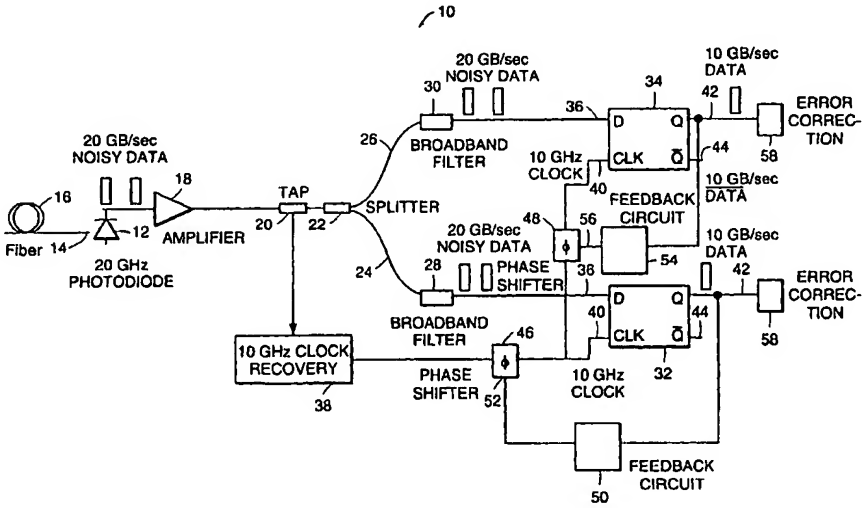
(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

[Continued on next page]

(54) Title: DEMULTIPLEXER FOR HIGH DATA RATE SIGNALS



(57) Abstract: A demultiplexer for Time Division Multiplexed (TDM) signals is described. The demultiplexer includes an electrical splitter that separates an electrical TDM data signal into multiple electrical TDM data signals. A clock recovery circuit generates a clock signal that is synchronized to the electrical TDM data signal and that has a frequency that is harmonically related to a single TDM channel data rate. A phase shifter adjusts the phase of the clock signal. The demultiplexer also includes multiple decision circuits each having a data input for receiving the electrical TDM data signal. Each of the decision circuits also has a clock input that is electrically coupled to an output of the clock recovery circuit for receiving the clock signal. Each of the decision circuits generates demultiplexed TDM signals. The phase shifter is adjusted so that the desired data in each of the demultiplexed TDM signals is selected.

WO 02/49248 A2

Published:
— *without international search report and to be republished upon receipt of that report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

Demultiplexer for High Data Rate Signals

Field of the Invention

[0001] The present invention relates generally to demultiplexing. In particular, the present invention relates to methods and apparatus for receiving and demultiplexing electrical and optical signals.

Background of the Invention

[0002] Optical receivers for optical fiber communication systems convert modulated optical signals received at the output end of the optical fiber into received electrical data signals. Optical receivers generally include a photodetector, an amplifier, a demodulator and other signal processing circuitry. A photodetector, such as a photodiode, is optically coupled to the end face of the optical fiber. The photodetector converts the received modulated optical signal into an electrical data signal. The amplifier amplifies the received optical signal to a level that is large enough for electronic processing.

[0003] The design of the demodulator depends on the modulation format used by the optical communication system. In intensity modulated direct detection optical communication systems, the received signal is in the form of optical pulses representing 1 and 0 bits and it is converted directly into an electric current. Demodulation is typically done by a decision circuit that identifies bits as 1 or 0 depending on the amplitude of the electrical current. The accuracy of the decision circuit depends on the signal-to-noise ratio of the electrical signal generated by the photodetector.

[0004] The modulated optical signals are transmitted over an optical fiber where they undergo attenuation and dispersion. In addition, optical amplifiers in the communication link add significant noise to the optical signals. Some prior art optical receivers use high-speed decision circuits to "clean" eye data that is corrupted by amplitude and phase noise.

[0005] Optical Time-Division Multiplexing (OTDM) communication systems can transmit data in a single optical channel at ultra-high bit rates. Functionally OTDM is identical to electronic TDM. Bits associated with different channels are interleaved in the time domain to form a bit interleaved bit stream. In operation, OTDM transmitters multiplex several lower-speed optical bit streams modulated at bit rate R to form a bit interleaved optical bit stream modulated at bit rate RN, where N is the number of multiplexed optical channels. OTDM receivers receive the bit interleaved optical bit stream at bit rate NR and extract the lower-speed optical bit streams modulated at bit rate R.

[0006] OTDM transmitters and receivers use high-speed multiplexing and demultipexing techniques. OTDM multiplexing is described in U.S. patent application serial number 09/566,303, entitled Bit Interleaved Optical Multiplexing, which is assigned to the current assignee. The entire disclosure of U.S. patent application serial number 09/566,303 is incorporated herein by reference. OTDM demultiplexers demultiplex individual channels from an OTDM signal. There are several electro-optical and all-optical demultiplexing techniques known in the art. OTDM demultiplexers require a clock signal that is a periodic pulse train having a frequency that is harmonically related to a single channel bit rate. The clock signal is an electrical clock signal for electro-optic demultiplexing, and is an optical pulse train for all-optical demultiplexing.

[0007] Some prior art demultiplexers are electro-optic and use Mach-Zehnder-type lithium niobate modulators. Each modulator in the demultiplexer halves the bit rate by rejecting alternate bits in the incoming signal. Other prior art demultiplxers are all-optical. State-of-the art OTDM receivers require all-optical demultiplexing because all-optical components are needed to process the high bit rates associated with the OTDM signals. One prior art all-optical demultiplxer uses nonlinear optical-loop mirrors constructed from a fiber loop whose ends are connected to two input ports of a fiber coupler. Still other prior art all-optical demultiplexers use four-wave mixing in a non-linear medium. These prior art electro-optic and all-optical OTMD demultiplexers are generally complex and difficult to implement.

Summary of the Invention

[0008] The present invention relates to receivers and demultiplexers for electronic Time Division Multiplexed (TDM) and Optical Time Division Multiplexed (OTDM) communication systems. One advantage of demultiplexers and receivers of the present invention is that they are relatively simple and easy to implement. In one embodiment, a demultiplexer of the present invention uses decision circuits for demultiplexing TMD and OTMD signals.

[0009] Accordingly, the present invention features a demultiplexer for demultiplexing high-speed signals. In one embodiment, the demultiplexer demultiplexes Time Division Multiplexed (TDM) signals. The demultiplexer includes an electrical splitter that separates an electrical TDM data signal into a plurality of electrical TDM data signals that propagate in a plurality of electrical transmission lines. A broadband filter may be coupled to at least one of the plurality of electrical transmission lines to filter noise from the TDM data signal. Filters may also be coupled to at least one of the plurality of electrical transmission lines to shape and broaden the pulse to increase more link margin.

[0010] A clock recovery circuit generates a clock signal that is synchronized to the electrical TDM data signal and that has a frequency that is harmonically related to the TDM channel data rate. Harmonically related is defined herein to mean frequencies that are equal to the single channel TDM channel data rate, a sub-harmonic of the single TDM channel data rate, or an integer multiple of the single channel TDM channel data rate. In one embodiment, the clock recovery circuit includes a harmonic mixer, phase detector, and a voltage controlled oscillator. The voltage controlled oscillator may be a dielectric resonator oscillator.

[0011] A phase shifter adjusts the phase of the clock signal. In one embodiment, the demultiplexer includes a plurality of phase shifters. In this embodiment, a respective one of the plurality of phase shifters is electrically coupled between the output of the clock recovery circuit and the clock input of a respective one of a plurality of decision circuits used for demultiplexing. In one embodiment, header and SONET information is used to control the state of the phase shifter.

[0012] The demultiplexer also includes a plurality of decision circuits. Each of the

plurality of decision circuits has a data input that is electrically coupled to one of the plurality of electrical transmission lines. The data input receives the electrical TDM data signal. Each of the plurality of decision circuits also has a clock input that is electrically coupled to an output of the clock recovery circuit. The clock input receives the clock signal. Each of the plurality of decision circuits generates demultiplexed TDM signals at a data output. The phase shifter is adjusted so that the desired data in each of the demultiplexed TDM signals is selected. In one embodiment, header or SONET information is used to control the state of the phase shifter.

[0013] In one embodiment, the demultiplexer includes a feedback circuit that has an input electrically coupled to a data output of at least one of the plurality of decision circuits. An output of the feedback circuit is electrically coupled to a control input of the phase shifter. The feedback circuit generates a signal at the output that is related to the phase of the demultiplexed TDM signal generated by the decision circuit. The signal causes the phase shifter to adjust the phase of the clock signal propagated to the decision circuit so that the desired demultiplexed TDM data signal generated by the decision circuit is selected.

[0014] In one embodiment, the demultiplexer includes an error correction circuit that has an input that is electrically coupled to the data output of one of the plurality of decision circuits. The error correction circuit may be a forward error correction (FEC) circuit.

[0015] The present invention also features a method of demultiplexing TDM data signals. The method includes splitting an electrical TDM data signal into a plurality of electrical TDM data signals. In one embodiment, the electrical TDM data signal is derived from an OTDM data signal. The OTDM data signal may comprise a return-to-zero (RZ) OTDM data signal. The electrical TDM data signals may be filtered to reduce noise.

[0016] A clock signal is generated that is synchronized to the electrical TDM data signal and that has a frequency that is harmonically related to a single TDM channel data rate. Each of the plurality of electrical data signals is propagated though one of a plurality of decision circuit that is clocked with the clock signal, thereby generating a

plurality of demultiplexed TDM signals.

[0017] A phase of the clock signal to at least one of the plurality of decision circuits is then adjusted so that desired data in at least one of the plurality of demultiplexed TDM signal is selected. In one embodiment, the phase of the clock signal to each of the plurality of decision circuits is adjusted so that each of the plurality of demultiplexed TDM signal is selected. Also, in one embodiment, the phase of the clock signal is adjusted by sampling a portion of the at least one of the plurality of demultiplexed TDM signals and adjusting the phase of the clock signal relative to an amplitude or BER of the sampled portion of the demultiplexed TDM signal.

[0018] In addition, the present invention features an Optical Time Division Multiplexed (OTDM) receiver. The receiver includes a detector that is positioned to receive an OTDM data signal. The detector generates an electrical TDM data signal that is indicative of the OTDM data signal. In one embodiment, the OTDM data signal is received from an optical fiber communication link.

[0019] In one embodiment, the detector comprises a photodiode having a bandwidth that is substantially greater than the bandwidth of the OTDM data signal. In one embodiment, an amplifier is electrically coupled to an output of the detector. The amplifier amplifies the electrical TDM data signal to useful signal levels. Typically, the bandwidth of the amplifier is greater than the bandwidth of the electrical TDM data signal.

[0020] The receiver includes an electrical splitter that separates an electrical TDM data signal into a plurality of electrical TDM data signals that propagate in a plurality of electrical transmission lines. A broadband filter may be coupled to at least one of the plurality of electrical transmission lines to filter noise from the TDM data signal. A clock recovery circuit generates a clock signal that is synchronized to the electrical TDM data signal and that has a frequency that is harmonically related to a single TDM channel data rate. The clock recovery circuit may include a harmonic phase detector. The clock recovery circuit may also include a dielectric resonator oscillator.

[0021] A phase shifter adjusts the phase of the clock signal. In one embodiment, the receiver includes a plurality of phase shifters. In this embodiment, a respective

one of the plurality of phase shifters is electrically coupled between the output of the clock recovery circuit and the clock input of a respective one of a plurality of decision circuits.

[0022] The receiver also includes a plurality of decision circuits. Each of the plurality of decision circuits has a data input that is electrically coupled to one of the plurality of electrical transmission lines. The data input receives the electrical TDM data signal. Each of the plurality of decision circuits also has a clock input that is electrically coupled to an output of the clock recovery circuit for receiving the clock signal. In addition, each of the plurality of decision circuits generates demultiplexed TDM signals at a data output. The phase shifter is adjusted so that the desired data in each of the demultiplexed TDM signals is selected.

[0023] In one embodiment, the receiver includes a feedback circuit that has an input electrically coupled to a data output of at least one of the plurality of decision circuits. An output of the feedback circuit is electrically coupled to a control input of the phase shifter. The feedback circuit generates a signal related to the phase of the demultiplexed TDM signal generated by the decision circuit and causes the phase shifter to adjust the phase of the clock signal propagated to the decision circuit so that the bit error rate is reduced.

Brief Description of the Drawings

[0024] This invention is described with particularity in the appended claims. The above and further advantages of this invention may be better understood by referring to the following description in conjunction with the accompanying drawings, in which like numerals indicate like structural elements and features in various figures. The drawings are not necessarily to scale, emphasis instead being placed upon illustrating the principles of the invention.

[0025] Fig. 1 illustrates an optical receiver that uses decision circuits according to the present invention.

[0026] Fig. 2 illustrates a clock recovery circuit according to the present invention for the optical receiver of Fig. 1.

Detailed Description

[0027] Fig. 1 illustrates an optical receiver 10 that uses decision circuits according to the present invention. The receiver 10 includes a photodiode 12 that is in optical communication with an optical data source. The optical data source may be an optical RZ data source. In one embodiment, the receiver 10 receives data transported though an optical fiber communication link. In this embodiment, the photodiode 12 is in optical communication with the end face 14 of an optical fiber 16. The photodiode 12 converts the received optical data signal into an electrical data signal. The photodiode 12 typically has a response time that is fast enough to convert substantially all of the useful optical data to an electrical data signal.

[0028] In long-haul optical communication systems, the converted electrical data signal is a relatively low-level signal. In addition, the converted electrical data signal contains substantial noise that may result in loss of data. An electronic amplifier 18 amplifies the electrical data signal to useful signal levels. In one embodiment, the electronic amplifier 18 is a broadband electronic amplifier that has a bandwidth wide enough to capture substantially all of the useful electrical data. A RF coupler 20 samples a portion of the electrical data signal for clock recovery. In one embodiment, the RF coupler 20 is a broadband optical coupler that passes substantially all of the useful data.

[0029] A splitter 22 separates the electrical data signal into a first and a second electrical data signal that propagate in a first 24 and second electrical transmission lines 26, respectively. In one embodiment, a first 28 and a second filter 30 is electrically coupled to each of the first 24 and the second waveguide 26, respectively. The first 28 and second filter 30 are broadband filters that reject high frequency noise that may erroneously trigger the decision circuits.

[0030] The receiver 10 includes a clock recovery circuit 38 that includes a phase lock loop that locks onto the tone from the electrical data signal. The clock recovery circuit 38 receives a portion of the electrical signal from the RF coupler 20 and generates a clock signal having a frequency that is harmonically related to the single channel bit rate and that is synchronized or locked to the received optical data signal.

[0031] The receiver 10 includes a first 32 and a second decision circuit 34. The

output of the first 28 and the second filter 30 is electrically coupled to a data input 36 of the first 32 and the second decision circuit 34. The output of the clock recovery circuit 38 is electrically coupled to the clock input 40 of the first 32 and the second decision circuit 34. The first 32 and the second decision circuit 34 includes a data output 42 that generates a demultiplexed data stream having a data rate that is one-half the data rate of the received optical data signal. In one embodiment, at least one of the first 32 and the second decision circuit 34 includes a complementary data output 44 that generates a complementary demultiplexed data stream that has a data rate that is one-half the data rate of the received optical data signal.

[0032] The first 32 and the second decision circuit 34 may be any type of decision circuit. There are numerous commercially available decision circuits. The decision circuits 32, 34 remove amplitude and phase noise and generally clean the output data and the complementary output data. In one embodiment, the decision circuits 32, 34 include a D flip/flop. The decision circuits 32, 34 may also include a wide-band data amplifier that improves sensitivity. Commercially available decision circuits according to the present invention having specified maximum data rate that are less than the data rate of the electrical data signal have been shown to operate according to the present invention.

[0033] In one embodiment, a first phase shifter 46 is electrically coupled between the clock recovery circuit 38 and the clock input 40 of the first decision circuit 32. A second phase shifter 48 is electrically coupled between the output of the first phase shifter 46 and the clock input 40 to the second decision circuit 34. The first phase shifter 46 modifies the phase of the clock signal to select the desired demultiplexed data stream and complementary demultiplexed data stream generated by the first decision circuit 32. The second phase shifter 48 modifies the phase of the clock signal to select the desired demultiplexed data stream and complementary demultiplexed data stream generated by the second decision circuit 34. In other embodiments, the clock recovery circuit 38 includes a phase shifter.

[0034] In one embodiment, a feedback circuit 50 is electrically coupled between a control input 52 of the first phase shifter 46 and the data output 42 of the first decision circuit 32. The feedback circuit 50 samples a portion of the data output from the first decision circuit 32 and generates a feedback signal that instructs the phase shifter 46

to select the desired demultiplexed data stream and complementary demultiplexed data stream. In addition, the feedback circuit 50 may generate a feedback signal that instructs the phase shifter 46 to reduce the bit error rate. In other embodiment, the feedback circuit 50 is electrically coupled between the control input 52 of the first phase shifter 46 and the complementary data output 44 of the first decision circuit 32.

[0035] Similarly, in one embodiment, a feedback circuit 54 is electrically coupled between a control input 56 of the second phase shifter 48 and the data output 42 of the second decision circuit 34. The feedback circuit 54 samples a portion of the data output from the second decision circuit 34 and generates a feedback signal that instructs the phase shifter 48 to select the desired demultiplexed data stream and complementary demultiplexed data stream. In addition, the feedback circuit 54 may generate a feedback signal that instructs the phase shifter 48 to lower the bit error rate. In other embodiments, the feedback circuit 54 is electrically coupled between the control input 56 of the second phase shifter 48 and the complementary data output 44 of the second decision circuit 34.

[0036] In one embodiment, error correction circuits 58 are electrically coupled to the data output 42 of the first 32 and second decision circuit 34. The error correction circuit 58 detects and corrects errors in the demultiplexed signal. The error correction circuit 58 may be a forward error correction (FEC) circuit. Error correction circuits 58 may also be electrically connected to the complementary data output 44 of the first 32 and second decision circuit 34. In other embodiments, error detection circuits are used and an error signal if feedback to the transmitter.

[0037] The operation of the optical receiver 10 can be further explained with an example of demultiplexing a 20GB/sec TMD data signal, such as a RZ data signal. The type of data signal and data rates presented in the example are given only for purposes of illustrating the invention and do not limit the invention in any way. In one embodiment of the invention, the optical receiver 10 demultiplexes a 20GB/sec TMD data signal into two 10GB/sec data channels. The photodiode 12 detects the 20GB/sec RZ data stream and converts it into a 20GB/sec electrical data signal. The photodiode 12 has a bandwidth that is sufficient to detect useful data in a 20GHz signal. The 20 GB/sec electrical data signal is amplified by the amplifier 18, which has a bandwidth great enough to amplify the useful data.

[0038] A 10GHz clock is recovered using the clock recovery circuit 38. The phase lock loop locks onto the 20GHz tone from the electrical data signal. In one embodiment, the clock recovery circuit 38 includes a 10GHz dielectric resonant oscillator and a harmonic phase detector that is configured in a feedback loop, as described in connection with the clock recovery circuit 100 of Fig. 2.

[0039] The recovered clock signal is split and transmitted to the clock input 40 of the first 32 and the second decision circuit 34 with the appropriate phase, so that every other data bit from the 20GB/sec data stream is clocked out of the Q data port of the decision circuits 32, 34. In this way, the data is demultiplexed from a single 20GB/sec data stream to two 10GB/sec data streams. Decision circuits having maximum data rates that are significantly less than the data rate of the RZ data signal can be used for performing substantially error-free demultiplexing.

[0040] Fig. 2 illustrates a clock recovery circuit 100 according to the present invention. The clock recovery circuit 100 includes a narrow-band amplifier 102 that amplifies the electrical data signal. In addition, the clock recovery circuit 100 includes a Phase Lock Loop (PLL) 104. The PLL 104 synchronizes or locks the frequency and phase of a local oscillator onto the frequency and phase of data on a single TDM channel. In one embodiment, the PLL 104 is a linear PLL. The PLL includes a Phase Detector (PD) 106 or phase comparator, a Loop Filter (LF) 108, and a Voltage Controlled Oscillator (VCO) or Dielectric Resonant Oscillator (DRO) 110.

[0041] The PLL 104 includes a phase detector 106 that has a first input 112 that receives the filtered electrical data signal and a second input 114 that receives a signal from the VCO 110. The phase detector 106 compares the phase of the electrical data signal with the phase of the signal generated by the VCO or DRO 110 and generates at an output 116 a signal that includes a DC component and a superimposed AC component. The DC component is proportional to the phase error between the electrical data signal and the signal generated by the VCO or DRO 110.

[0042] In one embodiment, the phase detector 106 is a harmonic mixer. A harmonic mixer is a three-port device that includes a nonlinear element. The harmonic mixer mixes the electrical data signal with a local oscillator signal and generates an error signal that has a DC component and a superimposed AC

component. The DC component of the error signal has a magnitude that is proportional to the phase error.

[0043] The PLL 104 includes a loop filter 108 that has an input 118 that is electrically connected to the output 116 of the phase detector 106. The loop filter 108 filters the error signal generated by the phase detector 106 and passes the filter signal to an output 120. In one embodiment, the loop filter 108 is a low pass lead-lag loop filter that includes a phase leading and phase lagging filter network. The phase leading network controls the dampening of the PLL 104. The loop filter 108 may be an active filter that has gain greater than one. In this embodiment, the loop filter 108 substantially cancels the AC component of the signal generated by the phase detector 106.

[0044] The VCO 110 has a control input 122 that is electrically connected to the output 120 of the loop filter 108. The VCO 110 generates a local oscillator signal that has a frequency, which is determined by the magnitude of the error signal. In one embodiment, the VCO 110 is a Dielectric Resonator Oscillator (DRO). In other embodiments, the clock recovery circuit 100 includes a Current Controlled Oscillator (CCO).

[0045] In operation, when the frequency and phase of the VCO or DRO is synchronized or locked onto the frequency and phase of data on a single TDM channel, the phase error between the output signal of the VCO or DRO and the reference signal is substantially zero or a constant. If a phase error accumulates, the PLL 104 changes the frequency and/or phase of the oscillator so that the phase error is reduced to a minimum, thereby synchronizing or locking the phase of the output signal to the phase of the reference signal.

Equivalents

[0046] While the invention has been particularly shown and described with reference to specific preferred embodiments, it should be understood by those skilled in the art that various changes in form and detail may be made therein without departing from the spirit and scope of the invention as defined by the appended claims. For example, the demultiplexer and receiver of the present invention can be used with electronic communication systems as well as optical communication

systems. Also, although the invention was described in connection with demultiplexing TDM data signals, the methods and apparatus of the present invention can be used to demultiplex numerous other types of high data rate signals.

[0047] What is claimed is:

1. A demultiplexer comprising:

a. an electrical splitter that separates an electrical data signal into a plurality of electrical data signals that propagate in a plurality of electrical transmission lines;

b. a clock recovery circuit that generates a clock signal that is synchronized to the electrical data signal and that has a frequency that is harmonically related to a single channel data rate;

c. a phase shifter that adjusts the phase of the clock signal; and

d. a plurality of decision circuits, each of the plurality of decision circuits having a data input that is electrically coupled to one of the plurality of electrical transmission lines, the data input receiving the electrical data signal, a clock input that is electrically coupled to an output of the clock recovery circuit, the clock input receiving the clock signal, and a data output that generates a demultiplexed signal,

wherein the phase shifter adjusts the phase of the clock signal to at least one of the plurality of decision circuits to select desired data to be demultiplexed.

2. The demultiplexer of claim 1 wherein the electrical data signals comprise time division multiplexed (TDM) data signals.

3. The demultiplexer of claim 1 wherein the phase shifter adjusts the phase of the clock signal to at least one of the plurality of decision circuits so that a bit error rate of at least one of the demultiplexed signals is reduced.

4. The demultiplexer of claim 1 wherein the phase shifter is adjusted so a bit error rate in at least one of the demultiplexed signals is minimized.

5. The demultiplexer of claim 1 wherein the phase shifter comprises a plurality of phase shifters, a respective one of the plurality of phase shifters is electrically coupled between the output of the clock recovery circuit and the clock input of a respective one of the plurality of decision circuits.

6. The demultiplexer of claim 1 further comprising a feedback circuit that has an input electrically coupled to a data output of at least one of the decision circuits and an output that is electrically coupled to a control input of the phase shifter, the feedback circuit generating a signal related to a bit error rate of at least one of the demultiplexed signals and causing the phase shifter to adjust a phase of the clock signal propagated to at least one of the plurality of decision circuits.

7. The demultiplexer of claim 1 further comprising a forward error correction circuit that includes an input that is electrically coupled to the data output of one of the plurality of decision circuits, the forward error correction circuit correcting errors in the demultiplexed signal.

8. The demultiplexer of claim 1 wherein the clock recovery circuit includes a dielectric resonator oscillator.

9. The demultiplexer of claim 1 further comprising a broadband filter that filters the electrical data before the electrical data is demultiplexed by one of the plurality of decision circuits.

10. A method of demultiplexing data signals, the method comprising:

a. splitting an electrical data signal into a plurality of electrical data signals;

b. generating a clock signal that is synchronized to the electrical data signal and that is harmonically related to a single channel data rate;

c. propagating a respective one of the plurality of electrical data signals though a respective one of a plurality of decision circuits, each of the plurality of decision circuits being clocked with the clock signal, thereby generating a plurality of demultiplexed signals; and

d. adjusting a phase of the clock signal to at least one of the plurality of decision circuits to select desired data in at least one of the plurality of demultiplexed signal.

11. The method of claim 10 wherein the data signal comprises a Time Division Multiplexed (TDM) data signal.

12. The method of claim 11 wherein the OTDM data signal comprises a return-to-zero (RZ) OTDM data signal.

13. The method of claim 12 further comprising converting an OTDM data signal into the electrical TDM data signal.

14. The method of claim 10 further comprising adjusting a phase of the clock signal to at least one of the plurality of decision circuits so that a bit error rate of data in the at least one of the plurality of demultiplexed signal is lower.

15. The method of claim 10 further comprising adjusting a phase of the clock signal to at least one of the plurality of decision circuits so that a bit error rate of data in the at least one of the plurality of demultiplexed signal is minimized.

16. The method of claim 10 wherein the adjusting the phase of the clock signal comprises adjusting a phase of the clock signal to each of the plurality of decision circuits so that desired data in each of the plurality of demultiplexed signal is selected.

17. The method of claim 10 wherein the adjusting the phase of the clock signal comprises sampling a portion of the at least one of the plurality of demultiplexed signals and adjusting the phase of the clock signal relative to the phase of the sampled portion of the demultiplexed signal.

18. The method of claim 10 further comprising filtering the electrical data signal to reduce noise.

19. An Optical Time Division Multiplexed (OTDM) receiver, the receiver comprising:

a. a detector that is positioned to receive an OTDM data signal, the detector generating an electrical TDM data signal indicative of the OTDM data signal;

b. a clock recovery circuit that generates a clock signal that is synchronized to the electrical TDM data signal and that has a frequency that is harmonically related to a single TDM channel data rate;

c. a phase shifter that adjusts the phase of the clock signal; and

d. a plurality of decision circuits, each of the plurality of decision circuits having a data input that is electrically coupled to one of the plurality of electrical transmission lines, the data input receiving the electrical data signal, a clock input that is electrically coupled to an output of the clock recovery circuit, the clock input receiving the clock signal, and a data output that generates a demultiplexed TDM signal,

wherein the phase shifter adjusts the phase of the clock signal to at least one of the plurality of decision circuits to select desired data to be demultiplexed .

20. The receiver of claim 19 wherein the phase shifter is adjusted so that a bit error rate of data in at least one of the demultiplexed TDM signals is reduced.

21. The receiver of claim 19 further comprising an amplifier that is electrically coupled to an output of the detector, the amplifier amplifying the electrical TDM data signal to useful signal levels.

22. The receiver of claim 21 wherein a bandwidth of the amplifier is greater than a bandwidth of the electrical TDM data signal.

23. The receiver of claim 19 wherein the OTDM data signal is received from an optical fiber communication link.

24. The receiver of claim 19 wherein the detector comprises a photodiode having a bandwidth that is substantially greater than the bandwidth of the OTDM data signal.

25. The receiver of claim 19 wherein the phase shifter comprises a plurality of phase shifters, a respective one of the plurality of phase shifters is electrically coupled between the output of the clock recovery circuit and the clock input of a respective one of the plurality of decision circuits.

26. The receiver of claim 19 further comprising a feedback circuit that has an input electrically coupled to a data output of at least one of the decision circuits and an output that is electrically coupled to a control input of the phase shifter, the feedback circuit generating a signal related to a bit error rate of at least one of the demultiplexed TDM signals and causing the phase shifter to adjusted a phase of the clock signal propagated to at least one of the plurality of decision circuits.

27. The receiver of claim 19 wherein the phase shifter is electrically coupled to the output of the clock recovery circuit.

28. The receiver of claim 19 wherein a maximum data rate of at least one of the plurality of decision circuits is less than a data rate of the TDM electrical data signal.

29. The receiver of claim 19 further comprising a broadband filter that filters the electrical data before the electrical data is demultiplexed by one of the plurality of decision circuits.

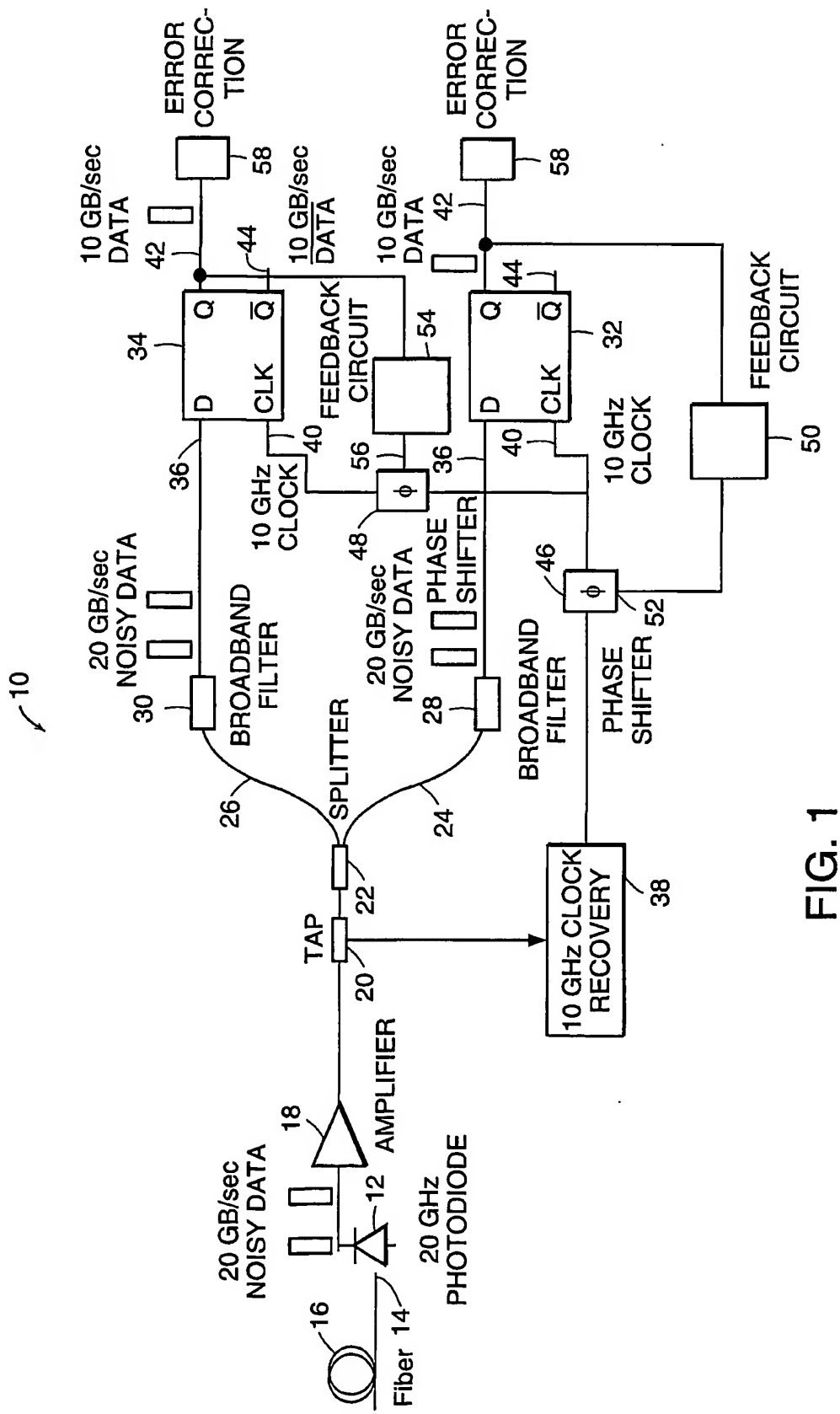

10
20 GB/sec NOISY DATA
16
Fiber
14
20 GHz PHOTODIODE
12
18
AMPLIFIER
20
TAP
22
SPLITTER
26
24
30
BROADBAND FILTER
28
BROADBAND FILTER
20 GB/sec NOISY DATA
20 GB/sec NOISY DATA
10 GHz CLOCK RECOVERY
38
PHASE SHIFTER
46
52
PHASE SHIFTER
48
10 GHz CLOCK
40
10 GHz CLOCK
36
36
56
φ
φ
FEEDBACK CIRCUIT
54
FEEDBACK CIRCUIT
50
34
D
CLK
Q
Q̄
32
D
CLK
Q
Q̄
42
10 GB/sec DATA
44
10 GB/sec DATA
10 GB/sec DATA
42
44
58
ERROR CORREC-TION
58
ERROR CORREC-TION

FIG. 1

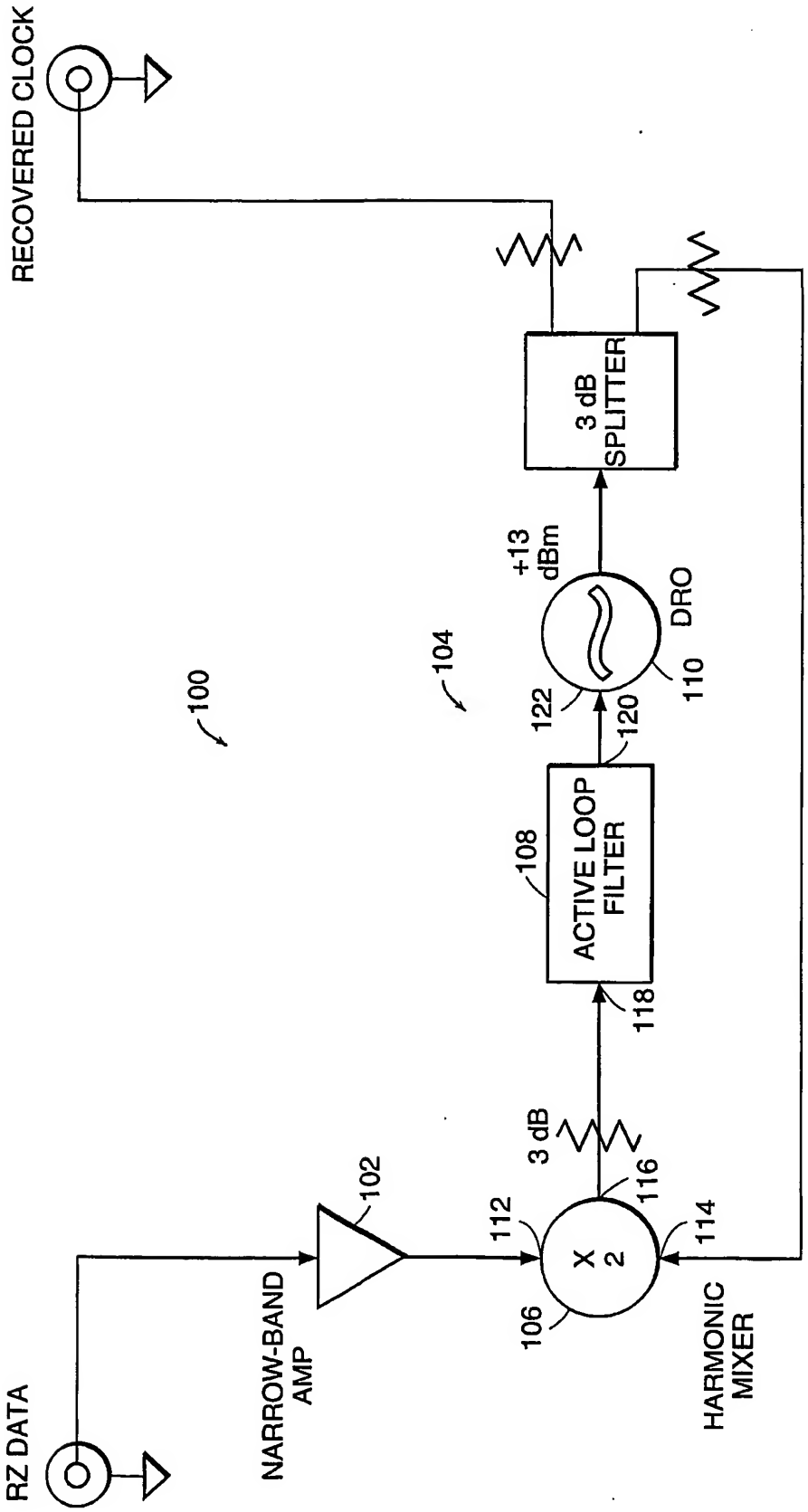

RECOVERED CLOCK
RZ DATA
NARROW-BAND AMP
HARMONIC MIXER
3 dB SPLITTER
+13 dBm
DRO
ACTIVE LOOP FILTER
3 dB
X 2
100
102
104
106
108
110
112
114
116
118
120
122

FIG. 2